

State-of-the-Art Physical Failure Analysis Capabilities



Nanolab Technologies offers Full Backside Preparation, Construction Analysis, Competitive Analysis, Cross-Section Preparation & Ultra High Resolution Documentation, Deprocessing, Decap, Deep UV Microscopy, Optical Microscopy, DualBeam FIBSEM, Root Cause Failure Analysis, FIB, SEM, and TEM Services.

Our Engineering Expertise combined with a State-of-the-Art Tool Set offers our customers an unparalleled one stop solution for comprehensive Failure Analysis.

For information or to arrange a demonstration please contact the New Pioneers in Failure Analysis:

Nanolab Technologies Incorporated
3833 North First Street
San Jose, CA 95134

Tel: 408-433-3320 Fax: 408-433-3321

DECAP

At Nanolab Technologies, we pride ourselves on the many types of decapsulation we can perform successfully. These include SOIC's, BGA's, COB's and custom packaging. We can also perform decap on devices that are still on Printed Circuit Boards or flexible circuits.

We also do delidding on a variety of packages. (CERDIP/Glass Lidded Packages, Custom Packages, etc.)

DEPROCESSING

Our deprocessing technique has been perfected to the level that we can inspect each layer individually and without inducing any defects. This is extremely important to ensure that what we find in your area of concern is truly the problem.

This technique can also be used to look at the circuitry of each layer when checking your first run of product that may be failing with no known reason. Were all of the correct masks used? Was a layer forgotten? We have seen examples of both of these cases in the past.

EMMI-FA

We can also do an inspection for damage from the backside of CSP's using this SOM4000. This is done non-invasively so it is the first step to take when you suspect EOS.

This technique can also be used to find hidden defects in a completed die – we thin the back of the package to die attach level, then remove the die attach and look at the die through the backside. We have found a crack in a die that was within the layers – neither visible from the top side (after decap) or on the silicon side. (The crack was subsequently verified by sectioning through the crack after detecting it with this technique.)

ROOT CAUSE FAILURE ANALYSIS

Nanolab Technologies is your one stop lab for a full Failure Analysis. From Electrical verification of the electrical signature to the final report after deprocessing or dual beam cross-section to show what caused the failure. The final report includes the documentation of each step used to find your anomaly/defect.

If you prefer, we can do the analysis by levels.

Level I usually includes x-ray, decap, internal visual inspection and a summary report. This is a good choice when you suspect EOS. Upon request, it can also include curve tracing to verify the electrical signature of the failure or CSAM if you suspect the device has suffered some thermal excursion which might have delaminated the die from the package.

Level II is employed when nothing visible is found in Level I. It usually includes EMMI/Laser Scan to find the failing area and either deprocessing, dual beam FIB or a combination of both to find the anomaly/defect causing the failure. A final report shows the documentation at each step employed during the analysis.

